CLAIMS

1. A method for erasing a target memory sector, said target memory sector having a plurality of memory blocks, each of said plurality of memory blocks having a plurality of core memory cells, each of said plurality of core memory cells being capable of storing a first bit and a second bit, said target memory sector further having a first edge column, said first edge column being shared by a first neighboring memory cell, said first neighboring memory cell being capable of storing a third bit and a forth bit, said method comprising the steps of:

pre-programming said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks;

pre-programming one of said third bit and said fourth bit of said first neighboring memory cell;

erasing said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks.

2. The method of claim 1, further comprising programming said one of said third bit and said fourth bit of said first neighboring memory cell after said erasing step.

3. The method of claim 2, further comprising over-erase correcting said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks after said erasing step.

4. The method of claim 1, further comprising:

pre-programming the other one of said third bit and said fourth bit of said first neighboring memory cell prior to said erasing step;

programming said other one of said third bit and said fourth bit of said first neighboring memory cell after said erasing step.

5. The method of claim 1, wherein said one of said third bit and said fourth bit of said first neighboring memory cell is adjacent to said first edge column.

6. The method of claim 1, wherein at least one of said plurality of memory blocks is a repaired block, said target memory sector further including a redundant block having a plurality of redundant memory cells, each of said plurality of redundant memory cells being capable of storing a fifth bit and a sixth bit, said redundant block further having a second edge column, said second edge column being shared by a second neighboring memory cell, said second neighboring memory cell being capable of storing a seventh bit and an eighth bit, said method further comprising:

pre-programming one of said seventh bit and said eighth bit of said second neighboring memory cell;

wherein said erasing step further comprises erasing said fifth bit and said sixth bit of said plurality of redundant memory cells of said redundant block.

7. The method of claim 6, further comprising programming said one of said

seventh bit and said eighth bit of said second neighboring memory cell after said erasing step.

8. The method of claim 6, wherein said repaired block includes a plurality of repaired memory cells, each of said plurality of repaired memory cells capable of storing a ninth bit and a tenth bit, said method further comprising pre-programming at least one of said ninth bit and said tenth bit of at least one of said plurality of repaired memory cells prior to said erasing step.

9. The method of claim 8, further comprising programming said at least one of said ninth bit and said tenth bit of said at least one of said plurality of repaired memory cells after said erasing step.

10. A method for erasing a target memory sector, said target memory sector having a plurality of memory blocks, each of said plurality of memory blocks having a plurality of core memory cells, each of said plurality of core memory cells being capable of storing a first bit and a second bit, said target memory sector further having a first edge column and a second edge column, said first edge column being shared by a first neighboring memory cell, said first neighboring memory cell being capable of storing a third bit and a forth bit, said second edge column being shared by a second neighboring memory cell, said second neighboring memory cell being capable of storing a fifth bit and a sixth bit, said method comprising the steps of:

pre-programming said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks;

erasing said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks;

programming said one of said third bit and said fourth bit of said first neighboring memory cell after said erasing step;

programming said one of said fifth bit and said sixth bit of said second neighboring memory cell after said erasing step.

11. The method of claim 10, further comprising:

pre-programming one of said third bit and said fourth bit of said first neighboring memory cell prior to said erasing step;

pre-programming one of said fifth bit and said sixth bit of said second neighboring memory cell prior to said erasing step.

12. The method of claim 10, wherein at least one of said plurality of memory blocks is a repaired block, said target memory sector further including a redundant block having a plurality of redundant memory cells, each of said plurality of redundant memory cells being capable of storing a seventh bit and an eighth bit, said redundant block further having a third edge column and a fourth edge column, said third edge column being shared by a third neighboring memory cell, said third neighboring memory cell being capable of storing a ninth bit and a tenth bit, said fourth edge

column being shared by a fourth neighboring memory cell, said fourth neighboring memory cell being capable of storing an eleventh bit and a twelfth bit, wherein said erasing step further comprises erasing said seventh bit and said eighth bit of said plurality of redundant memory cells of said redundant block, said method further comprising:

pre-programming one of said ninth bit and said tenth bit of said third neighboring memory cell;

pre-programming one of said eleventh bit and said twelfth bit of said fourth neighboring memory cell;

programming said one of said ninth bit and said tenth bit of said third neighboring memory cell after said erasing step;

programming said one of said eleventh bit and said twelfth bit of said fourth neighboring memory cell after said erasing step.

13. The method of claim 12, wherein said repaired block includes a plurality of repaired memory cells including a first repaired memory cell and a second repaired memory cell, each of said plurality of repaired memory cell being capable of storing a thirteenth bit and a fourteenth bit, wherein said first repaired memory cell is capable of storing fifteenth bit and a sixteenth bit, said second repaired memory cell is capable of storing a seventeenth bit and an eighteenth bit, said method further comprising:

pre-programming one of said fifteenth bit and a sixteenth bit of said first repaired memory cell prior to said erasing step;

pre-programming one of said seventeenth bit and an eighteenth bit of said second edge memory cell prior to said erasing step;

programming said one of said fifteenth bit and a sixteenth bit of said first edge memory cell after said erasing step;

programming said one of said seventeenth bit and an eighteenth bit of said second edge memory cell after said erasing step.

14. The method of claim 12, wherein said repaired block includes a plurality of repaired memory cells, each of said plurality of repaired memory cell capable of storing a thirteenth bit and a fourteenth bit, said method further comprising pre-programming said thirteenth bit and said fourteenth bit of said plurality of repaired memory cells prior to said erasing step.

15. The method of claim 14, further comprising programming said thirteenth bit and said fourteenth bit of said plurality of repaired memory cells after said erasing step.

16. A method for erasing a target memory sector, said target memory sector having a plurality of memory blocks, each of said plurality of memory blocks having a plurality of core memory cells, each of said plurality of core memory cells being capable of storing a first bit and a second bit, said target memory sector further having a first edge column, said first edge column being shared by a first neighboring memory

cell, said first neighboring memory cell being capable of storing a third bit and a forth bit, said method comprising pre-programming said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks, said method further comprising erasing said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks, said method being characterized by:

pre-programming one of said third bit and said fourth bit of said first neighboring memory cell prior to said erasing step.

17. The method of claim 16, further comprising programming said one of said third bit and said fourth bit of said first neighboring memory cell after said erasing step.

18. The method of claim 17, further comprising over-erase correcting said first bit and said second bit of said plurality of core memory cells of said plurality of memory blocks after said erasing step.

19. The method of claim 16, wherein at least one of said plurality of memory blocks is a repaired block, said target memory sector further including a redundant block having a plurality of redundant memory cells, each of said plurality of redundant memory cells being capable of storing a fifth bit and a sixth bit, said redundant block further having a second edge column, said second edge column being shared by a second neighboring memory cell, said second neighboring memory cell being capable of storing a seventh bit and an eighth bit, said method further comprising:

pre-programming one of said seventh bit and said eighth bit of said second neighboring memory cell;

wherein said erasing step further comprises erasing said fifth bit and said sixth bit of said plurality of redundant memory cells of said redundant block.

20. The method of claim 19, further comprising programming said one of said seventh bit and said eighth bit of said second neighboring memory cell after said erasing step.